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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,000	10/17/2003	Masayuki Furumiya	NEC 03FN026	4404

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,000	FURUMIYA ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *14-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-6, 8-9, 12-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Terayama et al (U.S. 6,541,840).

As to claim 1, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device comprising: a first conductivity type semiconductor substrate (82) connected to a first power supply ("VCC"); a second conductivity type semiconductor layer (comprising elements 81, 83) provided on the first conductivity type semiconductor substrate (82), the second conductivity type semiconductor (81, 83) being connected to a second power supply ("GND"); and a device forming portion (forming portion of "PMOS" or "NMOS") provided on the second conductivity type semiconductor layer (comprising elements 81, 83), a

decoupling capacitor [see the decoupling capacitor mounted between the P-well and N-well regions as shown in figure 8b] formed at an interface between the first conductivity type semiconductor substrate (82) and the second conductivity type semiconductor layer (comprising elements 81, 83).

As to claim 2, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the second conductivity type semiconductor layer (comprising elements 81, 83) is provided on an entire top surface of the first conductivity type semiconductor substrate (82), and a bottom surface of the first conductivity type semiconductor substrate (82) is connected to the first power supply ("VCC").

As to claim 3, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the device forming portion has a first conductivity type well ("N-well") contacting the second conductivity type semiconductor layer (comprising elements 81, 83) and connected to a third power supply (Vss, Figure 6c) and another decoupling capacitor [see a decoupling capacitor mounted between N-well and P-well regions as shown in figure 8c] is formed at an interface between the first conductivity type well ("N-well") and the second conductivity type semiconductor layer (comprising elements 81, 83).

As to claim 4, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein device forming portion has: another second conductivity type semiconductor layer (see "P-well region" on left side of the structure as shown in figure 8c) electrically connected to the second conductivity type semiconductor layer (comprising elements 81, 83), and a first conductivity type well ("N-well") provided on the another second conductivity type semiconductor layer (see "P-well region" on left side of the semiconductor

integrated circuit device) contacted with the another second conductivity type semiconductor layer and connected to a third power supply (Vss, figure 6c), and another decoupling capacitor (see a decoupling capacitor mounted between N-well and P-well regions) is formed at an interface between the first conductivity type well (N-well") and the another second conductivity type semiconductor layer (see "P-well region" on left side of the structure as shown in figure 8c).

As to claim 5, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the device forming portion (forming portion of "PMOS" or "NMOS") has an active element ("PMOS" or "NMOS") connected to the third power supply (Vss, Fig. 6b).

As to claim 6, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein a potential of the third power supply (Vss, Fig. 6b or Fig. 7b) differs from potentials of the first and second power supplies ("Vcc" and "GND", figure 8b).

As to claim 8, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the second conductivity type semiconductor layer (comprising elements 81, 83) is locally provided on a top surface of the first conductivity type semiconductor substrate (82) [*applicant should note that: a bottom surface of substrate 82 will become a top surface if the apparatus in figure 8(b) is rotated up side down*], the device forming portion (forming portion of "PMOS" or "NMOS") is formed in a region on the top surface of the first conductivity type semiconductor substrate (82) where the second conductivity type semiconductor layer (comprising elements 81, 83) is not provided, and the first conductivity type semiconductor substrate (82) is connected to the first power supply (Vcc") via the device forming portion (forming portion of "PMOS" or "NMOS").

As to claim 9, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the device forming portion (forming portion of "PMOS" or "NMOS") has a first conductivity type well ("N-well") and the first conductivity type semiconductor substrate (82) is connected to the first power supply ("Vcc") via the first conductivity type well ("N-well").

As to claim 12, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the second conductivity type semiconductor layer (comprising 81, 83) is connected to the second power supply ("GND") via the device forming portion (forming portion of "PMOS" or "NMOS").

As to claim 13, Terayama et al discloses in figures 8(b) and 8(c) a semiconductor integrated circuit device, wherein the device forming portion (forming portion of "PMOS" or "NMOS") has a second conductivity type well ("P-well") and the second conductivity type semiconductor layer (81, 83) is connected to the second power supply ("GND") via the second conductivity type well ("P-well").

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terayama et al (U.S. 6,541,840) in view of Disney (U.S. 6,768,171).

As to claim 11, Terayama et al does not disclose a semiconductor integrated circuit device wherein the substrate body has a resistivity of 100 Ω-cm or higher.

Disney discloses in figure 7A a semiconductor integrated circuit device wherein the substrate body has a resistivity of 100 Ω-cm or higher ("100-150 ohm/cm") (see col. 8, lines 60-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Terayama et al by having a substrate body has a resistivity of 100 Ω-cm or higher as taught by Disney for providing a proper charge balance among the alternating p-type and n-type layers that are formed in the device.

5. Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terayama et al (U.S. 6,541,840) in view of Kawaguchi et al (U.S. 6,259,136).

As to claims 7 and 10, Terayama et al does not disclose the first conductivity type semiconductor substrate has: a substrate body, and a surface portion having a lower resistivity than that of the substrate body.

Kawaguchi et al (U.S. 6,259,136) discloses in figure 3 a semiconductor integrated circuit device, wherein first conductivity type semiconductor substrate (11) has: a substrate body (including 14), and a surface portion (15) having a lower resistivity than that of the substrate body (including 14) (see col. 5, lines 58-64). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor integrated circuit device of Terayama et al by having the first conductivity type semiconductor substrate has: a substrate body, and a surface portion having a lower resistivity than that of the

substrate body as taught by Kawaguchi et al for providing a high performing conductivity type semiconductor substrate.

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that Terayama does not teach a device forming portion provided on a second conductivity type semiconductor layer which is provided on a first type semiconductor layer and a capacitor formed between the first and second semiconductor layers.

In response, the examiner disagrees with applicant's argument because figures 8(b)-8(c) clearly disclose: a device forming portion (forming portion of "PMOS" or "NMOS") provided on a second conductivity type semiconductor layer (comprising elements 81, 83) which is provided on a first type semiconductor layer (82), and a capacitor (see the decoupling capacitor mounted between the P-well and N-well regions as shown in figure 8b) formed between the first and second semiconductor layers (82, 81 & 83).

Since the claimed invention is "read on" the structure of Terayama et al, applicant's arguments have been fully considered but they are not persuasive.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
5/1/08